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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/801,350	03/07/2001	Chun Hsiang Lai	JCLA6643	4896

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EXAMINER

NADAV, ORI

ART UNIT PAPER NUMBER

2811

DATE MAILED: 07/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Applicant No.

09/801,350

Applicant(s)

LAI ET AL.

Examiner

Vori nadav

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 April 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) 5-12 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4 and 13 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Quigley (5,781,388).

Quigley teaches in figure 1 an electrostatic discharge (ESD) protection circuit, suitable for use on the I/O pad, the ESD protection circuit comprising: a silicon controlled rectifier (SCR) circuit 22, which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively connected to the I/O pad and a ground voltage Vss, so as to discharge the electrostatic charges; and

an anti-latch-up circuit RC 17, 18, which comprises a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal 21, respectively coupled to a voltage source (the pad line), the ground voltage Vss, and the third connection terminal of the SCR circuit, wherein the sixth connection terminal of the anti-latch-up circuit 21 is directly connected to the third connection terminal of the SCR circuit, whereby an anti-latch-up voltage signal is sent from the sixth connection terminal to the SCR circuit, for

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preventing latching up of the SCR circuit during normal operation, wherein SCR circuit is triggered by an ESD event.

Although Yu does not state a voltage source, this feature is inherent in Quigley's device as the line connected to the pad is the voltage source to the device. Furthermore, capacitor C also provides a voltage source to the device. Note that the device would not function without a voltage source.

2. Claims 1, 3, 4 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin (5,982,601).

Lin teaches in figure 9 and related text an electrostatic discharge (ESD) protection circuit, suitable for use on the I/O pad, the ESD protection circuit comprising: a silicon controlled rectifier (SCR) circuit (see figure 6 for clarity), which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively connected to the I/O pad (Anode) and a ground voltage (Cathode), so as to discharge the electrostatic charges; and

an anti-latch-up circuit 51, which comprises a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal A, respectively coupled to a voltage source (the pad line), the ground voltage, and the third connection terminal of the SCR circuit, wherein the sixth connection terminal of the anti-latch-up circuit A is directly connected to the third connection terminal of the SCR circuit, whereby an anti-latch-up voltage signal is sent from the sixth connection terminal to the SCR circuit, for

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preventing latching up of the SCR circuit during normal operation, wherein SCR circuit is triggered by an ESD event.

Regarding claim 3, Lin teaches in figure 5 an SCR circuit comprises: a P-type substrate; an N well, formed in the p-type substrate; a first P+ doped region, formed in the P-type substrate and coupled to the ground voltage GND; a first N+ doped region, formed in the P-type substrate, adjacent to the first P+ doped region, and coupled to the ground voltage GND; a second N+ doped region, formed between the P-type substrate and the N well, adjacent to the first N+ doped region, and coupled via the third connection terminal of SCR circuit to the sixth connection terminal of the anti-latch-up circuit A, serving as a guard ring to collect electrons to avoid latch up when the anti-latch-up circuit sends signal through the sixth connection terminal to the third connection terminal of the SCR circuit during normal operation, and floating when the anti-latch-up circuit sends no signal to the SCR circuit during an ESD event;

a second P+ doped region, formed in the N well, adjacent to the second N+ doped region, and coupled to the I/O pad 1; and a third N+ doped region, formed in the N well, adjacent to the second P+ doped region, and coupled to the voltage source (the pad line).

Regarding claim 4, Lin teaches in figure 6C an anti-latch-up circuit comprises: a capacitor C, having a first contact end and a second contact end, respectively coupled to the second N+ doped region and the ground voltage, and a resistor R, having a first

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end and a second end, respectively coupled to the voltage source and the second N+ doped region.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Quigley or Lin in view of Ker et al. (5,754,380).

Quigley and Lin teach substantially the entire claimed structure, as applied to claim 1 above, except a first diode, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and a second diode, having a first input end and a second input end, respectively connected to the I/O pad and a voltage source.

Ker et al. teach in figure 1 a first diode 70, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and a second diode 60, having a first input end and a second input end, respectively connected to the I/O pad and a voltage source.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first diode, having a first input end and a second input end,

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respectively connected to the ground voltage and the I/O pad; and a second diode, having a first input end and a second input end, respectively connected to the I/O pad and a voltage source in Quigley and Lin's device in order to provide better protection for the device against ESD event.

### ***Response to Arguments***

5. Applicant argues that prior art does not teach the amendment to claim 1 "wherein an operating voltage is supplied to the anti-latch up circuit regardless of an ESD event"

Claim 1 was not amended to include the limitations "wherein an operating voltage is supplied to the anti-latch up circuit regardless of an ESD event". Claim 1 was amended to include the limitations "whereby an anti-latch-up signal is sent from the sixth connection terminal to the SCR circuit for preventing latching up of the SCR circuit during normal operation, wherein SCR circuit is triggered by an ESD event".

6. Applicant argues on page 7 that the voltage divider of Quiley is not directly connected to a voltage source as required by the claimed invention.

The limitations of a voltage divider being directly connected to a voltage source is not recited in the claim 1. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

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7. Applicant argues that Quiley and Lin do not teach an SCR circuit being triggered by an ESD event, because the SCR circuit is triggered by the voltage divider 17, 18.

During an ESD event, the device, including the SCR circuit, is subjected to a sudden surge of voltage, and thus the SCR circuit will be triggered.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.



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Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is (571) 272-1660. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is 308-0956



O.N.  
June 29, 2004

ORI NADAV  
PATENT EXAMINER  
TECHNOLOGY CENTER 2800